REMARKS / ARGUMENTS

Claims 1-57 are pending in the instant application. Claims 1-6, 14, 16-20, 28, 29, 35-37, 49 and 55-56 have been cancelled. Claims 7-13, 15, 21-27, 30-34, 38-48, 50, 51 and 57 are rejected.

Claims 55-56 have been objected to for allegedly substantially duplicating claims 52-53, and have been cancelled to remove the objection.

Claims 51 and 57 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ting-Chung Chen, U.S. Patent No. 6,108,047 (hereinafter, Chen)

Claims 7-13, 15, 40-48, and 50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,452,235, issued to Isani (hereinafter, Isani), in view of U.S. Patent No. 5,812,144, issued to Potu et al. (hereinafter, Potu). Claims 21-27, 30-34, and 38-39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Potu. Claims 52-54 are allowed.

The Applicant respectfully submits that the claims define patentable subject matter and traverses these rejections at least based on the following remarks.

I. EXAMINER'S RESPONSE TO ARGUMENTS IN THE OFFICE ACTION

In the Office Action at pages 12, regarding claim 7 and 40, the Examiner disagrees with the Applicant that neither Isani nor Potu discloses a "clock selection

circuitry that receives and selects one of the video input clock and the display output clock for upscaling". The Examiner relies for support on Potu in the abstract, alleging that the enable logics (Y_en, UV_en), which are used for controlling (time-interleaving) the active display components (Y, U or V) relative to the clock signal (U_clk) in the bus enable logic circuit 54, is used for clock selection. In other words, the Examiner seems to imply that the enable logics, namely the Y_en and the UV_en, are clock selection logics to select one of the video input clock and a display output clock for downscaling and upscaling.

The Applicant respectfully disagrees and points out that Potu, in both the abstract, and in Figs. 2-3, discloses that the **bus enable logics (Y_en, UV_en) are for time-interleaving Y, U or V components for an output to the encoder 42**. Specifically, Potu discloses that time-interleaving is carried out by alternately interleaving a U or a V component at gate 1 with a Y component at gate 2 during every U_clk cycle. Therefore, **Potu does not disclose or suggest that the Y_en, UV_en enable logics are for clock selection**, as asserted by the Examiner. In fact, **there is no clock to be selected, since Potu discloses that the U_clk is the only clock** in the bus enable logic 54. Accordingly, since the Y_en and the UV_en, are not clock selection logics, Potu's bus enable logic circuit 54 is not a clock selection circuitry.

In addition, the Examiner relies for support on Potu in col. 6, lines 18-60 to argue that Potu discloses scaling using a pixel clock (PCLK) (asserted as the

video input clock by the Examiner), and a frequency adjusted pixel clock (asserted as the display output clock by the Examiner). In other words, the Examiner seems to assert that Potu discloses or suggests that the Y_en, UV_en enable logics are used to select between a PCLK (as video input clock) and a frequency adjusted pixel clock (as display output clock) for scaling.

The Examiner is referred to the Applicant's initial argument that the Y_en, UV_en enable logics does not select any clock, they are for time-interleaving the Y, U or V components. Therefore, the Examiner's argument of selecting one of the PCLK (asserted as the video input clock by the Examiner) and a frequency adjusted pixel clock (asserted as the display output clock by the Examiner) for scaling is moot.

Moreover, the Examiner fails to point out specifically which frequency adjusted pixel clock is referred to as a display output clock, since Potu discloses that the pixel clock PCLK (asserted as the video input clock by the Examiner) is used to generate a plurality of synchronized clock signals: namely the PCLKB4 (1/4 of PCLK), PCLKB2 (1/2 of PCLK) for downscaling (see col. 6, lines 18-21), and the UV_FMRE* and Y_ FMRE* for upscaling (see col. 6, lines 59-60). Potu clearly does not disclose or suggest that each of these clock signals (i.e. PCLKB2, PCLKB4, UV_FMRE* and Y_ FMRE*), are used as a display output clock at all. In fact, Potu never mentions the use of any display output clock.

Assuming for the sake of argument, that the Examiner's alleged bus enable logic 54 disclosed by Potu is the same as the Applicant's clock selection circuitry (which it is not), Potu still does not disclose "clock-selection circuitry that receives a video input clock and a display output clock," as recited by the Applicant in claim 7. Potu's Fig. 2 clearly discloses that the bus enable logic 54 receives at the input: a U_clk, the enable logics (i.e. Y_en, UV_en), and the Y, U and V components. There is no disclosure that the bus enable logic 54 (asserted as clock selection circuitry by the Examiner) receives a video input clock (asserted as the PCLK by the Examiner) and a display output clock (asserted as the PCLKB2, PCLKB4, UV_FMRE* and Y_ FMRE* by the Examiner). Therefore, Potu's bus enable logic 54 is not the "clock selection circuitry," as recited in claim 7 by the Applicant.

Therefore, based on the above rationale, the Applicant maintains that Potu does not disclose or suggest "clock-selection circuitry that receives a video input clock and a display output clock and selects one of the video input clock and the display output clock for upscaling and one of the video input clock and the display output clock for downscaling of the video image," as recited in claim 7 by the Applicant.

Finally, with regard to claim 7, the Examiner in page 13 of the Office Action relies for support in on col. 5, lines 4-7 and 10-15 of Potu, alleges that Potu teaches supplying synchronization signals to one of the field memory write downscale logic 46A or field memory read upscale logic 46B and storing the

scaled, thus disclosing "means for **determining whether** the video image is to be downscaled or upscaled".

The Applicant respectfully disagrees and points out that the Examiner's assertion contradicts with Potu's disclosure that the synchronized signals sent to one of the two scaling logics 46A or 46B, are for actual execution of downscaling or upscaling the video image. Potu does not disclose or suggest that the synchronized signals are for ascertaining or deciding (i.e. determining) whether to downscale or upscale the video image. Therefore Potu at best discloses or suggests "**means for scaling** the video image," but **not** "**means for determining whether** the video image is to be downscaled or upscaled." Therefore, the Applicant maintains that Potu does not disclose or suggest "means for **determining** whether the video image is to be downscaled or upscaled is to store the data," as recited in the Applicant's claim 7. Isani does not overcome the deficiencies of Potu.

II. OBJECTION TO CLAIMS 55-56

Claims 55-56 have been objected to for allegedly substantially duplicating claims 52-53. The Applicant has cancelled claims 55-56 to remove the objection.

III. REJECTION UNDER 35 U.S.C. § 102

With regard to the anticipation rejections under 102(e), MPEP 2131 states that:

> "[a] claim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *See* MPEP at 2131 (internal citation omitted). Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See id.* (internal citation omitted).

A. Chen Does Not Anticipate Claims 51 and 57

The Applicant turns to the rejection of claims 51 and 57 under 35 U.S.C. § 102(e) as being anticipated by Chen. Without conceding that Chen qualifies as prior art under 35 U.S.C. 102(e), the Applicant respectfully traverses this rejection as follows.

A(1) Independent Claims 51 and 57

With regard to the rejection of independent claim 51 under 35 U.S.C. § 102(e), the Applicant submits that Chen does not disclose or suggest at least the limitation of "the scaler engine using a clock selected between a video input clock and a display output clock," as recited in the Applicant's claim 51.

In the Office Action, the Examiner asserts that Chen discloses the following:

> "Regarding independent claim 51 ... the scaler engine using a clock selected between a video input clock and a display output clock (Fig. 16 "148, 150");"

See the Office Action at page 3. The Examiner asserts that Chen's multiplier nodes 134 and 136 in Fig. 16A, are the same as the Applicant's scaler engine 52 in Figs 25-27. Based on this assertion, the Examiner alleges that Chen's multiplier nodes 134 and 136 **select between** the input clock signal 148 (asserted as a video input clock by the Examiner) and the output clock signal 150 (asserted as a display output clock by the Examiner) for scaling operations.

The Applicant respectfully disagrees and points out that in Fig. 16A, **Chen teaches using both the input clock signal 148 and the output clock signal 150 for scaling operation by the multiplier nodes 134 and 136**, instead of selecting between the input clock signal 148 and the output clock signal 150. The Examiner is referred to the following citation by Chen:

> "In schematic of FIG. 16A, data out signal 156 is received by D-type flipflop 130, which is clocked by input clock signal 148 to generate signal 158, which is applied to other D-type flipflop 132 and multiplier node 134. Flipflop 132 is clocked by input clock 148 to generate output signal received by multiplier node 136, which receives scale_2 signal 152 to generate output signal received by summing node 138. Multiplier node 134 also receives scale_1 signal 154 to apply output signal to summing node 138 to generate summed signal for another D-type flipflop 140, which is clocked by output clock signal 150 to generate output signal 160. As configured, memory address and control signals are generated in synchronization with input clock 148, two scale factors scale_1 signal 154 and scale_2 signal 152 are generated in synchronization with output clock 150, to generate scaled output 160 at desired output time."

See Chen at col. 12, lines 16-31. Chen in the above citation clearly teaches **using both the input clock signal 148 and output clock signal 150 for video scaling.** Specifically, Chen teaches that the scaling process requires using an input clock 148 to synchronize the memory address and to clock in data for scaling through the D-flipflops 130, 132. For the multiplier nodes 134 and 136, an output clock 150 is used to synchronize the scaling signals (scale_1 signal 154 and node 136 scale_2 signal 152). In other words, both the input clock signal 148 and the output clock signal 150 are both required, Chen does not disclose scaling using clock selection. Therefore, the Applicant maintains that Chen does not disclose or suggest at least the limitation of "**the scaler engine using a clock selected between a video input clock and a display output clock**," as recited in the Applicant's claim 51.

In addition, with regard to the rejection of independent claim 51 under 35 U.S.C. § 102(e), the Applicant submits that Chen does not disclose or suggest at least the limitation of "a memory capable of storing the video image or the first scaled video image," as recited in the Applicant's claim 51.

In the Office Action, the Examiner asserts that Chen discloses the following:

> "a memory capable of storing the video image or the first scaled video image (Fig. 16 "128")"

See the Office Action at page 3. The Examiner asserts that Chen in Fig. 16 discloses that the memory buffer 128 is capable of storing the input data 142 (asserted as the video image by the Examiner), and the first scaled video image (asserted as the output 160 in Fig. 16A, or output 190 in Fig. 16B). The Applicant respectfully disagrees and points out that Chen in both Figs. 16A and 16B shows that the outputs 160 or 190 have no return path to the memory buffer 128. Therefore, the Applicant maintains that Chen does not disclose or suggest at least the limitation of "a memory capable of storing the video image or the first scaled video image," as recited in the Applicant's claim 51.

Based on the foregoing rationale, the Applicant respectfully submits that claim 51 is not anticipated by Chen, and is allowable. The Applicant respectfully request that the rejection of claim 51 under 35 U.S.C. § 102(e) be withdrawn. Claim 57 is similar in many respects to independent claim 51, and therefore claim 57 is also allowable for the same rationale stated above with regard to claim 51. Furthermore, the Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 51 and 57 should such a need arise.

IV. REJECTION UNDER 35 U.S.C. § 103

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure, Rev. 6, Sep. 2007 ("MPEP") states the following:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See the MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" (citing *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007)). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

A. THE PROPOSED COMBINATION OF ISANI AND POTU DOES NOT RENDER CLAIMS 7-13, 15, 40-48, AND 50 UNPATENTABLE

The Applicant now turns to the rejection of claims 7-13, 15, 40-48, and 50 as being unpatentable over Isani in view of Potu.

A(1). Independent Claims 7 and 40

With regard to the rejection of independent claim 7 under 103(a), the Applicant submits that the combination of Isani and Potu does not disclose or suggest at least the limitation of "clock-selection circuitry that receives a video input clock and a display output clock and selects one of the video input clock and the display output clock for upscaling and one of the video input clock and the display output clock for downscaling of the video image," as recited by the Applicant in independent claim 7.

The Office Action concedes the following:

> However it is noted that Isani fails to disclose capable of both downscaling the video image to generate a first scaled video image and upscaling the video image to generate a second scaled video image, the scaler engine using a clock selected between a video input clock and a display output clock; and means for determining whether the video image is to be downscaled or upscaled.

See the Office Action at page 5. To address the deficiencies of Isani, the Examiner seeks support in Potu, and states the following:

> Potu discloses capable of both downscaling the video image to generate a first scaled video image and upscaling the video image to generate a second scaled video image (col. 5, lines 43-56), using a clock selected between a video input clock and a display output

> clock (col. 5, lines 50-52); and means for determining whether the video image is to be downscaled or upscaled (col. 5, lines 5-7).

See the Office Action in page 5. The Examiner relies on the following citations:

> "... What video adapter 22 provides is the ability to perform on-the-fiy resizing with pixel clock manipulation 50 of time-interleaved digital video component YVV data without requiring a separate scaling chip, additional buffers, or associated interface logic."

See Potu, col. 5, lines 50-52. In the Examiner's response to arguments section in the Office Action, the Examiner has separately cited Potu's abstract to allege that Potu's bus enable logic circuit 54 is the same as the Applicant's clock selection circuitry, and asserts that the enable logics (Y_en, UV_en) controls the selection of video input clock (asserted as the PCLK) and a display output (asserted as the Potu's frequency adjusted pixel clock.

The Applicant respectfully disagrees and refers the Examiner to Potu in the abstract:

> "The bus enable logic includes a clocked buffer, coupled to a U clock signal, a first enable gate, coupled in parallel to the clock buffer for passing either a U or V component of the digital video signal, and a second enable gate, coupled to a Y component of the digital video signal. The second enable gate is enabled by a Y enable signal and the bus enable log operates such that the Y component is active for two consecutive clock cycles and the U and V components alternate for the next two consecutive clock cycles such that in a given cycle period, two Y components are passed while one U and one V component are passed."

See Potu in the abstract. The Examiner relies for support on Potu in the abstract, alleging that the enable logics (Y_en, UV_en), which are used for controlling (time-interleaving) the active display components (Y, U or V) relative to the clock signal (U_clk) in the bus enable logic circuit 54, is used for clock selection. In other words, the Examiner seems to imply that the enable logics, namely the Y_en and the UV_en, are clock selection logics to select one of the video input clock and a display output clock for downscaling and upscaling.

The Applicant respectfully disagrees and points out that Potu, in both the abstract, and in Figs. 2-3, discloses that the **bus enable logics (Y_en, UV_en) are for time-interleaving Y, U or V components for an output to the encoder 42**. Specifically, Potu discloses that time-interleaving is carried out by alternately interleaving a U or a V component at gate 1 with a Y component at gate 2 during every U_clk cycle. Therefore, **Potu does not disclose or suggest that the Y_en, UV_en enable logics are for clock selection**, as asserted by the Examiner. In fact, **there is no clock to be selected, since Potu discloses that the U_clk is the only clock** in the bus enable logic 54. Accordingly, since the Y_en and the UV_en, are not clock selection logics, Potu's bus enable logic circuit 54 is not a clock selection circuitry.

In addition, the Examiner relies for support on Potu in col. 6, lines 18-60 to argue that Potu discloses scaling using a pixel clock (PCLK) (asserted as the video input clock by the Examiner), and a frequency adjusted pixel clock (asserted

as the display output clock by the Examiner). In other words, the Examiner seems to assert that Potu discloses or suggests that the Y_en, UV_en enable logics are used to select between a PCLK (as video input clock) and a frequency adjusted pixel clock (as display output clock) for scaling.

The Examiner is referred to the Applicant's initial argument that the Y_en, UV_en enable logics does not select any clock, they are for time-interleaving the Y, U or V components. Therefore, the Examiner's argument of selecting one of the PCLK (asserted as the video input clock by the Examiner) and a frequency adjusted pixel clock (asserted as the display output clock by the Examiner) for scaling is moot.

Moreover, the Examiner fails to point out specifically which frequency adjusted pixel clock is referred to as a display output clock, since Potu discloses that the pixel clock PCLK (asserted as the video input clock by the Examiner) is used to generate a plurality of synchronized clock signals: namely the PCLKB4 (1/4 of PCLK), PCLKB2 (1/2 of PCLK) for downscaling (see col. 6, lines 18-21), and the UV_FMRE* and Y_ FMRE* for upscaling (see col. 6, lines 59-60). Potu clearly does not disclose or suggest that each of these clock signals (i.e. PCLKB2, PCLKB4, UV_FMRE* and Y_ FMRE*), are used as a display output clock at all. In fact, Potu never mentions the use of any display output clock.

Assuming for the sake of argument, that the Examiner's alleged bus enable logic 54 disclosed by Potu is the same as the Applicant's clock selection circuitry (which it is not), Potu still does not disclose "**clock-selection circuitry** that **receives** a **video input clock and a display output clock**," as recited by the Applicant in claim 7. Potu's Fig. 2 clearly discloses that the bus enable logic 54 receives at the input: a U_clk, the enable logics (i.e. Y_en, UV_en), and the Y, U and V components. There is no disclosure that the bus enable logic 54 (asserted as clock selection circuitry by the Examiner) receives a video input clock (asserted as the PCLK by the Examiner) and a display output clock (asserted as the PCLKB2, PCLKB4, UV_FMRE* and Y_ FMRE* by the Examiner). Therefore, Potu's bus enable logic 54 is not the "clock selection circuitry," as recited in claim 7 by the Applicant.

Therefore, based on the above rationale, the Applicant maintains that Potu does not disclose or suggest "**clock-selection circuitry** that receives a **video input clock and a display output clock** and **selects one of the video input clock and the display output clock for upscaling** and **one of the video input clock and the display output clock for downscaling** of the video image," as recited in claim 7 by the Applicant.

With regard to the rejection of independent claim 7 under 103(a), the Applicant submits that the combination of Isani and Potu does not disclose or

suggest at least the limitation of "means for determining whether the video image is to be downscaled or upscaled," as recited by the Applicant in claim 7.

The Examiner relies for support in on col. 5, lines 4-7 and 10-15 of Potu, alleges that Potu teaches supplying synchronization signals to one of the field memory write downscale logic 46A or field memory read upscale logic 46B and storing the scaled, thus disclosing "means for **determining whether** the video image is to be downscaled or upscaled".

The Applicant respectfully disagrees and points out that the Examiner's assertion contradicts with Potu's disclosure that the synchronized signals sent to one of the two scaling logics 46A or 46B, are for actual execution of downscaling or upscaling the video image. Potu does not disclose or suggest that the synchronized signals are for ascertaining or deciding (i.e. determining) whether to downscale or upscale the video image. Therefore, Potu at best discloses or suggests "**means for scaling** the video image," but **not** "**means for determining whether** the video image is to be downscaled or upscaled." Therefore, the Applicant maintains that Potu does not disclose or suggest "means for **determining** whether the video image is to be downscaled or upscaled is to store the data," as recited in claim 7 by the Applicant. Isani does not overcome the deficiencies of Potu.

Accordingly, the proposed combination of Isani and Potu does not render independent claim 7 unpatentable, and a *prima facie* case of obviousness has not

been established. Independent claim 40 is similar in many respects to the method disclosed in independent claim 7. Therefore, the Applicant submits that independent claim 40 is also allowable over the references cited in the Office Action at least for the reasons stated above with regard to claim 7.

A(2). Rejection of Dependent Claims 8-13, 15, 41-48, and 50

Based on at least the foregoing, the Applicant believes the rejection of independent claims 7 and 40 under 35 U.S.C. § 103(a) as being unpatentable over Isani in view of Potu has been overcome and requests that the rejection be withdrawn. Additionally, claims 8-13 and 15 depend from independent claim 7, and claims 41-48 and 50 depend from independent claim 40. Therefore, claims 8-13, 15, 41-48, and 50 are, consequently, also respectfully submitted to be allowable.

In addition, with regard to claim 8, the Applicant has reviewed the cited reference (Isani at col. 3 lines 1-5), and submits that Isani shows that the video data from the video capture source 104 must pass through the video scalar 202 of the memory device 102. In other words, **only scaled video image** (in packed or planar format) are saved to the memory device in the FIFO 206, 208 and 210, and **only scaled video image** are received (output) from the memory to the MUX 212. Likewise, Potu does not show any means for determining whether the video image

is to be downscaled or upscaled since the synchronized signals are solely to carry out scaling functions (*See* Potu at col. 5, lines 5-7). Subsequently, Potu does not disclose "**outputting either the first scaled video image or the second scaled video image**." Therefore, the Applicant maintains that the combination of Isani and Potu does not disclose or suggest "providing the video image to be upscaled **or** the first scaled video image to the memory, ... providing the video image to be downscaled **or** the video image to be upscaled to the scaler engine, ... receiving the first scaled video image from the memory, receiving the second scaled video image from the scaler engine, and **outputting either the first scaled video image or the second scaled video image**," as recited in claim 8 by the Applicant. The Applicant submits that claim 8 should be allowable.

Regarding claim 9, the Applicant has reviewed the cited reference (Potu at col. 4 lines 63-67), and submits that Potu discloses that an analog video input CVBS is decoded by a video decoder 40 to generate digitized analog video components (Y, U, V). Potu does not disclose that the video input to the video decoder 40 is a digital video image. Therefore, the Applicant maintains that the combination of Isani and Potu does not disclose or suggest "fourth means capable of **receiving and selecting** between **a digital video image** and a digitized analog video image, and the fourth means outputs the **selected one of the digital video image** and the digitized analog video image as the video image," as recited in claim 9 by the Applicant. The Applicant submits that claim 9 should be allowable.

Regarding claim 11, the Applicant has reviewed the cited reference (Potu at col. 6 lines 28-60), and has pointed out that Potu has never disclosed that the downscale synchronized signals PCLKB2, PCLKB4, and upscale synchronized signals, UV_FMRE*, Y_ FMRE* are output display clock signals at all. Therefore, the Applicant maintains that the combination of Isani and Potu does not disclose or suggest "the scaler engine upscales the video image using the display output clock," as recited in claim 9 by the Applicant. The Applicant submits that claim 11 should be allowable.

Regarding claim 41-43, the Applicant submits that the same rationale of claim 8 applies, and therefore allowable.

Regarding claim 44, the Applicant submits that the same rationale of claim 9 applies, and therefore allowable.

Regarding claim 45-48 and 50, the Applicant submits that the same rationale of claims 10-13 and 15 applies, and therefore allowable.

B. Potu Does Not Render Claims 21-27, 30-34, and 38-39 Unpatentable

The Applicant now turns to the rejection of claims 21-27, 30-34, and 38-39 as being unpatentable over Potu.

B(1). Independent Claims 21 and 30

With regard to the rejection of independent claim 21 under 103(a), the Applicant submits that Potu does not disclose or suggest at least the limitation of "determining whether the video scaling engine requires less memory space to scale the video image before writing the video image to memory or after reading the video image from the memory," as recited by the Applicant in independent claim 21.

The Office Action states the following:

> Regarding claim 21, Potu discloses receiving a video image by a video scaling engine (col. 4, ll. 44-50); reducing memory space by scaling the video image before writing the video image to memory or after reading the video image from the memory (i.e. logic for determining whether to write the data to memory and downscale or read the data from memory and upscale, which provides for a reduction in bandwidth of the input data, which in turn requires less memory space as the reduction of data uses less memory space for storage) (col. 5, ll. 4-7, 10-15,43-45); and scaling the received video image based on the determination (col. 5, ll. 28-31; col. 6, ll. 22-24).

See the Office Action at pages 8-9. The Examiner cites the following:

> "Synchronization signals from video decoder 40 are also forwarded to field memory 46 through either field memory write and downscale logic 46A or field memory read and upscale logic 46B. These synchronization signals are further depicted in the various timing diagrams of FIGS. 3-5 and will be explained in greater detail in those particular figures."

See Potu at col. 5 lines 4-7. The Examiner seems to infer that the write downscale logic 46A and the read upscale logic 46B are logic for determining

whether to write the data to memory and downscale, or read the data from memory and upscale. The Applicant respectfully disagrees and submits that similar arguments, as used with respect to claim 7 above applies, namely, Potu discloses that the write downscale logic 46A is for downscaling video components (Y, U, V) by the generated synchronized signals PCLKB2, PCLKB4, and the read upscale logic 46B is for upscaling video components (Y, U, V) by the generated synchronized signals UV_FMRE*, Y_ FMRE*, as shown in Figs 3-5.

Moreover, the Applicant has reviewed the Examiner's citations, but is unable to find any disclosure or suggestion that Potu's write downscale logic 46A or the read upscale logic 46B performs the function of "determining whether the video scaling engine requires less memory space to scale the video image before writing the video image to memory or after reading the video image from the memory," as recited by the Applicant in independent claim 21. In fact, the Examiner's assertion contradicts with Potu's disclosure that the synchronized signals sent to one of the two scaling logics 46A or 46B, are for actual execution of downscaling or upscaling the video image. Potu does not disclose or suggest that the synchronized signals are for ascertaining or deciding (i.e. determining) whether to downscale or upscale the video image.

In addition, the Examiner relies for support on the following citation in Potu:

> "Video adapter 22, in this implementation, also provides a pass-through mode for putting out digital video data into field memory 46 without downsizing and read out the data from field memory 46 without upscaling."

See Potu at col. 5 lines 44-45. The Examiner again seems to infer that Potu's disclosure of a pass-through mode for putting out digital video data into field memory 46 without downsizing and read out the data from field memory 46 without upscaling is the same as "determining whether the video scaling engine requires less memory space to scale the video image before writing the video image to memory or after reading the video image from the memory," as recited by the Applicant in independent claim 21.

The Applicant again respectfully disagrees since Potu discloses that the pass through mode in fact by-pass any scaling (i.e. without downscaling, and without upscaling). Therefore the Applicant maintains that Potu's pass though mode is not "determining whether the video scaling engine requires less memory space to scale the video image before writing the video image to memory or after reading the video image from the memory," as recited by the Applicant in independent claim 21.

Therefore, based on the above rationale, the Applicant maintains that Potu does not disclose or suggest "determining whether the video scaling engine requires less memory space to scale the video image before writing the video image to memory or after reading the video image from the memory," as recited by the Applicant in independent claim 21.

Accordingly, Potu does not render independent claim 21 unpatentable, and a *prima facie* case of obviousness has not been established. Independent claim 30 is similar in many respects to the method disclosed in independent claim 21. Therefore, the Applicant submits that independent claim 30 is also allowable over the references cited in the Office Action at least for the reasons stated above with regard to claim 21.

B(2). Rejection of Dependent Claims 22-27, 31-34, and 38-39

Based on at least the foregoing, the Applicant believes the rejection of independent claims 21 and 30 under 35 U.S.C. § 103(a) as being unpatentable over Potu has been overcome and requests that the rejection be withdrawn. Additionally, claims 22-27 depend from independent claim 21, and claims 31-34 and 38-39 depend from independent claim 30. Therefore, claims 22-27, 31-34, and 38-39 are, consequently, also respectfully submitted to be allowable.

In addition, regarding claim 22-23 and 27 the Applicant has reviewed the cited reference (Potu at col. 5 lines 10-15), and submit that the same argument as used with regard to claim 21 above applies, namely, Potu does not disclose "determining if the video scaling engine requires less memory space to scale the video image before writing the video image to the memory...." Therefore, the Applicant submits that claims 22-23 and 27 should be allowable.

Regarding claims 30-33, the Applicant submits that the same argument as used with regard to claims 21-23 and 27 applies. Therefore, the Applicant submits that claims 30-33 should be allowable.

The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 22-27, 31-34, and 38-39.

CONCLUSION

Based on at least the foregoing, the Applicant believes that all claims 7-13, 15, 21-27, 30-34, 38-48, 50-54 and 57 are in condition for allowance. If the Examiner disagrees, the Applicant respectfully requests a telephone interview, and requests that the Examiner telephone the undersigned Patent Agent at (312) 775-8093.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

A Notice of Allowability is courteously solicited.

Respectfully submitted,

Date: June 02, 2008

/ Frankie W. Wong /

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